TEMIC

Siliconix

SUP/SUB40N06-25L

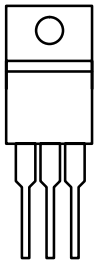
N-Channel Enhancement-Mode MOSFETs, Logic Level

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.022 @ V_{GS} = 10 V	40
	0.025 @ V_{GS} = 4.5 V	40

175° C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs

TO-220AB



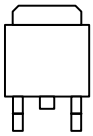
G D S

Top View

SUP40N06-25L

DRAIN connected to TAB

TO-263



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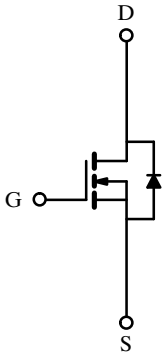
Top View

SUB40N06-25L



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	40	A
	T_C = 100°C		25	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current		I_{AR}	40	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	80	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	90[c]	W
	T_A = 25°C (TO-263)[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)		80	
Junction-to-Case		R_{thJC}	1.6	

Notes:
a. Duty cycle ≤ 1%.
b. See SOA curve for voltage derating.
c. Surface Mounted on FR4 Board, t ≤ 10 sec.

This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing,

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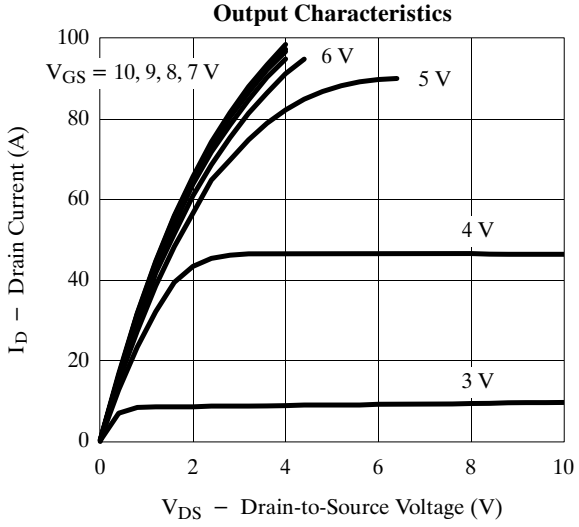
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125°C			50	
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 175°C			150	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			0.022	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125°C			0.043	
		V_{GS} = 10 V, I_D = 20 A, T_J = 175°C			0.053	
		V_{GS} = 4.5 V, I_D = 20 A			0.025	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 20 A				S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1800		pF
Output Capacitance	C_{oss}			350		
Reversen Transfer Capacitance	C_{rss}			100		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 40 A		40	60	nC
Gate-Source Charge[c]	Q_{gs}			9		
Gate-Drain Charge[c]	Q_{gd}			10		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.8 Ω I_D ≃ 40 A, V_{GEN} = 10 V, R_G = 2.5 Ω		10	20	ns
Rise Time[c]	t_r			9	20	
Turn-Off Delay Time[c]	$t_{d(off)}$			28	50	
Fall Time[c]	t_f			7	15	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				40	A
Pulsed Current	I_{SM}				100	
Forward Voltage[b]	V_{SD}	I_F = 40 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 40 A, di/dt = 100 A/µs		48	100	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			6		A
Reverse Recovery Charge	Q_{rr}			0.15		µC

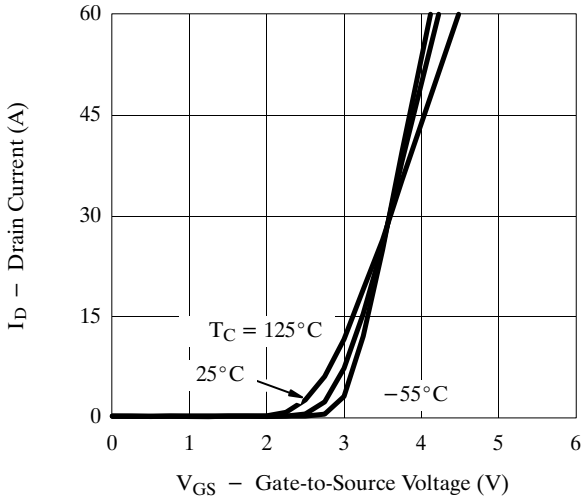
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

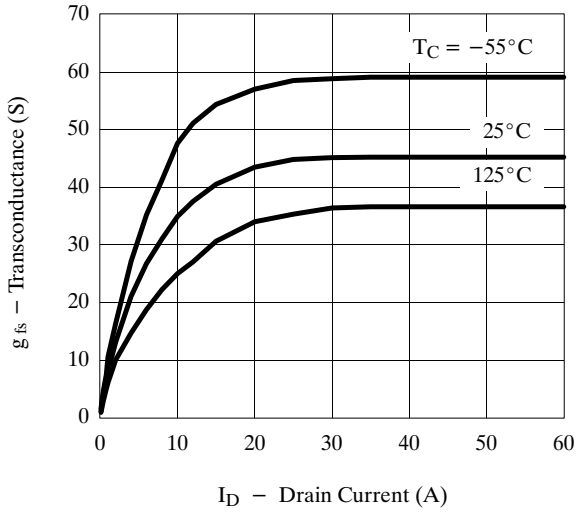
Output Characteristics



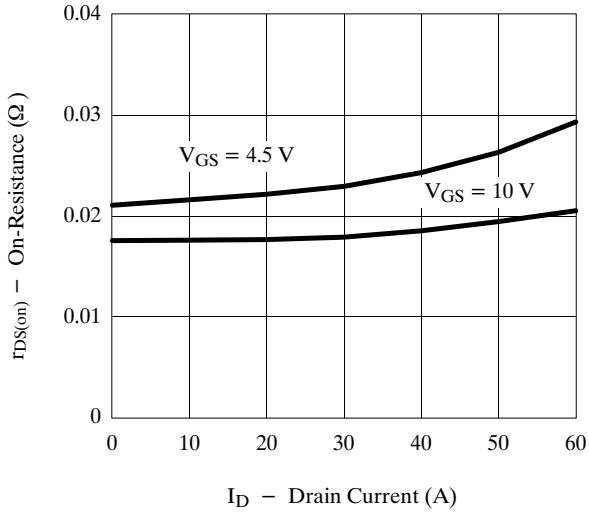
Transfer Characteristics



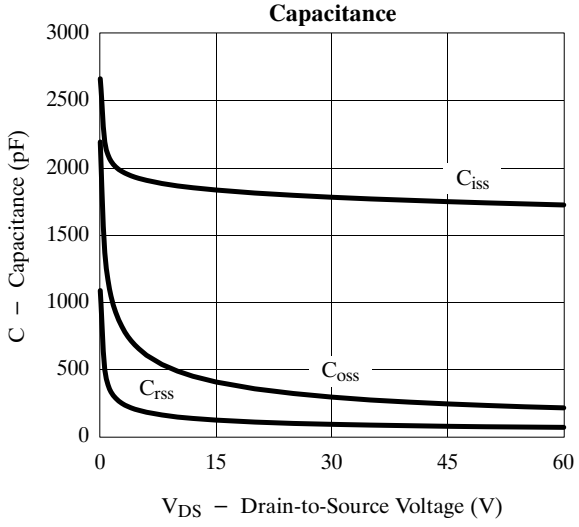
Transconductance



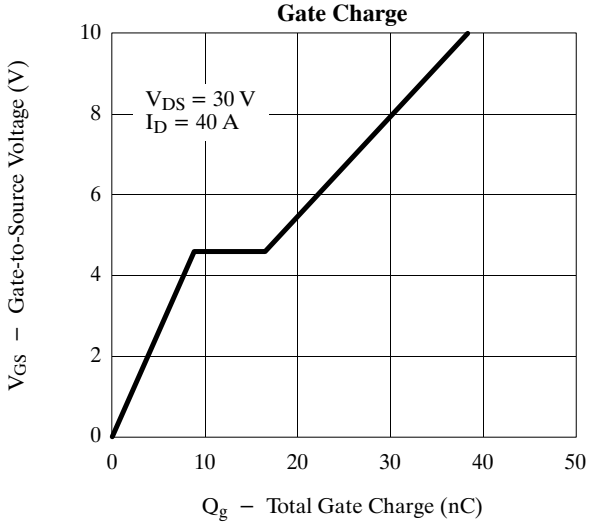
On-Resistance vs. Drain Current



Capacitance



Gate Charge



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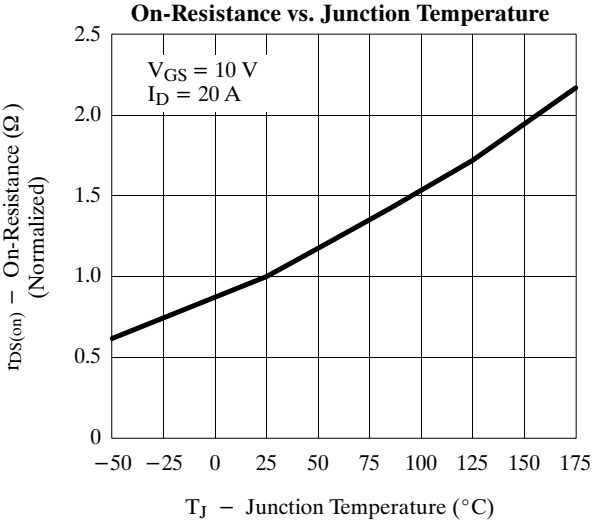
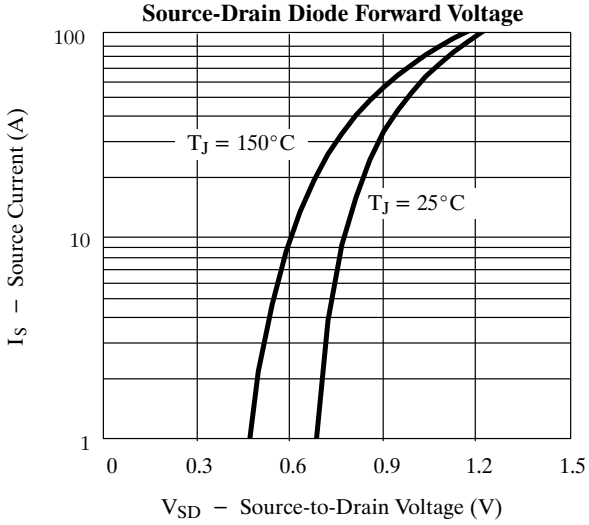
Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

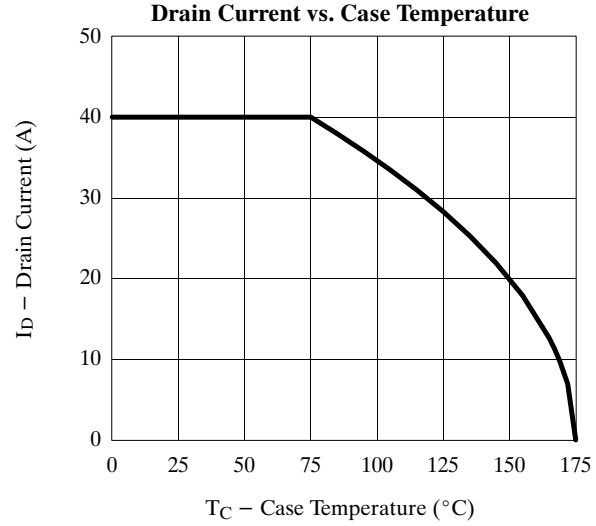


Source-Drain Diode Forward Voltage

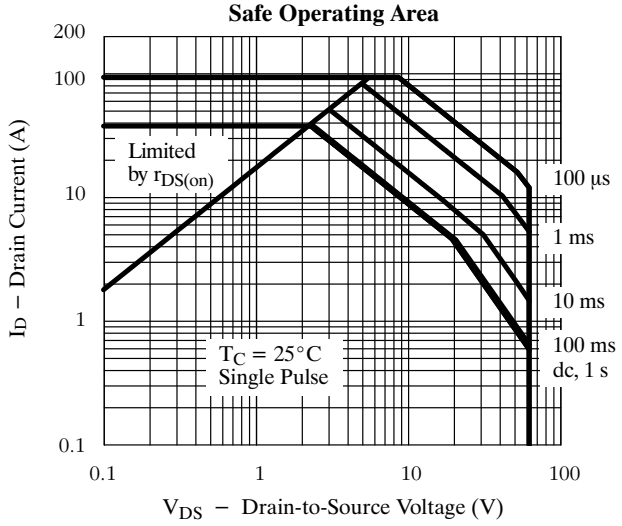


Thermal Ratings

Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case